

Single Event Upset Susceptibility Testing of the Xilinx *Virtex II* FPGA*

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Abstract

Heavy ion testing of the Xilinx *Virtex II* was conducted on the configuration, block RAM and user flip flop cells to determine their single event upset susceptibility using LETs of 1.2 to 60 MeVcm²/mg. A software program specifically designed to count errors in the FPGA is used to reveal $L_{1/e}$ values and single-event-functional interrupt failures.

I. INTRODUCTION

The Xilinx *Virtex II* FPGA is an advanced SRAM-configured, high gate- and pin-count device of current interest to many designers. The ability to reprogram and control the device while in operation however, make it especially favorable for use in space and avionic applications. Due to the architecture of FPGAs, the many static memory elements as well as their configuration memory array are susceptible to single event upsets that can lead to functional errors. Previously at MAPLD, results have been presented on the Xilinx *Virtex* FPGA that show sensitivity to upset of both the configuration and the user-incorporated memory elements when irradiated with heavy ions and protons meant to simulate the space radiation environment [1]. Thus, a test vehicle for SEU susceptibility measurements on the XQ2V1000FG256 has been developed and heavy ion test runs have been conducted at the Texas A&M Cyclotron on that bulk-CMOS for "static" configuration upsets.

II. EXPERIMENTAL DETAILS

A. Device Properties

The device chosen for this study is the *Virtex II*, XC2V1000. Device is a field programmable gate array procured as a commercial 256-pin wire-bond standard ball gate array (BGA) package. The *Virtex II* XC2V1000 is an SRAM based device that consists of 1M system gates with a core voltage of 1.5V. It is fabricated on a 0.15 μ m / 0.12 μ m CMOS 8-layer metal process and it's architecture optimized for high speed with low power consumption. This *Virtex II* includes 40 block RAMs, 432 maximum I/Os, and 4.1M configuration bits [2]. Devices were chemically etched on the top to expose the die and help improve ion range (Fig. 1).

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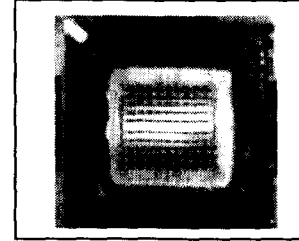


Figure 2: *Virtex II* XC2V1000 is etched to expose die to heavy ions. The individual blocks seen here are the internal configurable logic blocks (CLBS) situated among rows of block SelectRam, multipliers, input/output blocks (IOBs) and other *Virtex II* architectural components.

B. Irradiation Facility

Total dose irradiations were performed at the Cyclotron Institute's Radiation Effects Facility at Texas A & M University in College Station, Texas. Their facility consists of a set of high energy (25 MeV/nucleon) noble gas beams (Ne, Ar, Kr, and Xe) that provides a broad range of linear energy transfer (LET) (2-63 MeV/(mg/cm²)) and range penetration (254 to 790 microns). The ions used for this experiment are Neon, Argon, Krypton, and Xenon to obtain LETs from 1.21 – 61.3 MeV/(mg/cm²). All tests were performed in air with an eight-layer definition file put in.

C. Test Procedure

This SEU characterization of the *Virtex II* FPGA currently composes of three different static tests. The purpose of each of these tests was to determine the number of upsets in the configuration, block SelectRam and flip flops/latches cells in a more efficient manner with each successive test. The test platform for each test consisted of a *HW-AFXBG256-200* prototype board connected to the host PC and test software via Xilinx' MultiLinx cable or the Xilinx parallel III, JTAG cable (Fig. 2).

1) Static Configuration Memory Test

This test comprised of extracting only configuration upsets using Xilinx IMPACT device programming application to configure and verify the device through the parallel III JTAG IEEE cable. Immediately following after each beam run, 'verify' was performed to determine the number of differences in the configuration memory.

2) Static Configuration and Block SelectRam Test

The static configuration and block SelectRam test captures data through a MultiLinx cable connected directly to the DUT

through modifications made to the prototype board. A specifically designed C++ based application named FIVIT (Fault Injection and Verification Tool) test software was used to configure the DUT and readback SEUs in the memory cells. A screen capture of the program is included (Fig. 3). In addition, an HP6629A digital power supply was used to provide 3.3 V to the board and 1.5V to the FPGA. A separate laptop was connected to the HP6629A to strip chart the two voltage and current readings.

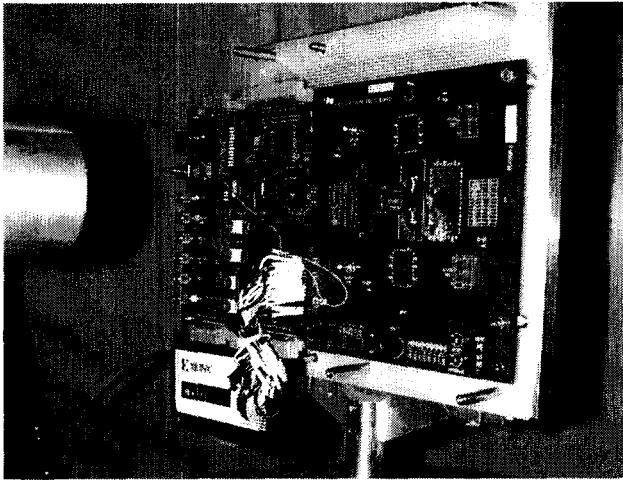


Fig. 2: HW-AFXBG256-200 prototype board connected to the host PC and test software via Xilinx' MultiLinx cable in front of beam at Texas A&M.

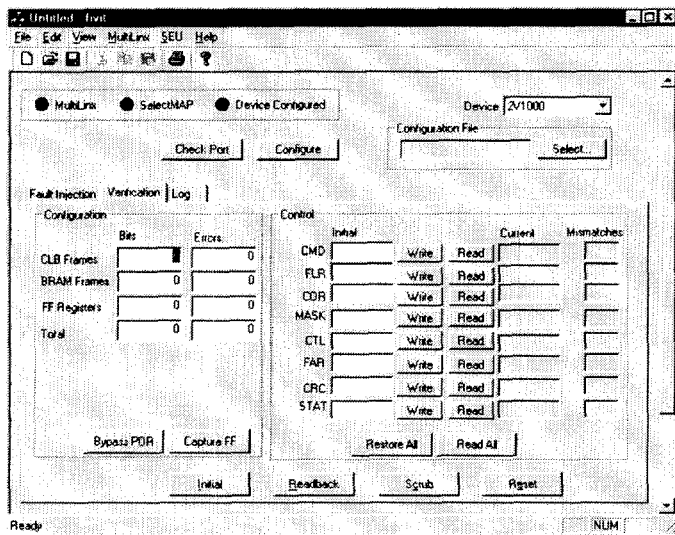


Figure 3: FIVIT (Fault Injection Verification Tool), a C++ based application used to check communication between the DUT and the software as well as determine the number of upsets in various memory cells and registers after each subsequent configuration and beam run.

3) Static Configuration, Block SelectRam & Flip-Flops

This last, and most current setup is identical to the static configuration and block SelectRam test above with the exception that more capabilities were added to FIVIT. New

features of FIVIT include the ability to set all flip-flops to either '1s' or '0s', capture their data, as well as read and write to configuration registers such as the command register (CMD), frame length register (FLR), configuration option register (COR), masking register for CTL (MASK), control register (CTL), frame address reader (FAR), CRC register, and the status register (STAT). Another useful utility added to FIVIT is the option of reading and writing to configuration registers through either the MultiLinx slave SelectMap mode or through the JTAG cable. This utility was incorporated as previous heavy ion tests revealed functional interrupts that disabled the SelectMap port.

III. TEST RESULTS

Each static test observed and counted upsets for one or more of the following elements: configuration memory, block SelectRam and user flip-flops and latches. In addition to upsets in these user elements, a number of single-event functional interrupts (SEFI) were noted. Heavy ions altering the logic states of the power-on-reset (POR) circuitry and SelectMap port were two of the more frequently occurring SEFIs, either disabling the communication between the FIVIT software or resetting the device. As more functionality was added to FIVIT with each successive test, greater visibility and control over the device was obtained and a few other types of SEFIs were discovered. More mention of this is made in sub-section "C. Static Configuration, block SelectRam & Flip-Flops Test."

A. Static Configuration Memory Test

The design implemented in the FPGA is a shift register design that automatically loads an alternating pattern until it is full. The capacity of the shift register used is (320x32) 9920 flip-flops. When verify is used in the 'IMPACT' program, the number of bit-flips in the configuration memory array is determined. The configuration memory cell SEU response is fitted to a physically based model presented by Larry Edmonds [3]. The equation used to fit the data is

$$\sigma = \sigma_{\text{sat}} \exp(-(L_{1/e}/\text{LET})) \quad (1)$$

where σ_{sat} (a fitting parameter) is the saturation cross-section and $L_{1/e}$ (another fitting parameter) is the LET at which the cross section is 1/e times the saturation cross-section. Under this model, the $L_{1/e}$ value for configuration memory cells was found to be approximately 5.5 MeVcm²/mg at a saturation cross section of 4.25 e-8 cm²/bit (Fig. 4). This $L_{1/e}$ value is slightly lower when compared to configuration memory bits at a later test. This is probably due to the lower range of LETs used to test the device as well as early test methods that had less visibility on the actual number of bits examined for upset.

B. Static Configuration and Block SelectRam Test

In this test method, FIVIT is implemented for the first time, used for measuring errors in the configuration memory and block SelectRam cells. SEFIs as a result of an ion hit to the POR and SelectMap circuitry were also identified through

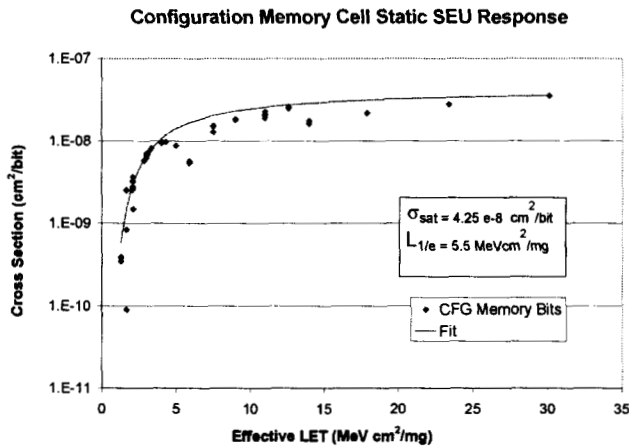


Figure 4: Cross-section vs. effective LET curve for configuration memory bits determined through the IMPACT program.

their failure signatures. As ions contact the device during the beam run, DUT current increased as errors were generated. A sudden decrease of the DUT current to its starting value would indicate a POR. Meanwhile, meaningless data in the configuration memory registers depicted a SelectMap error as communication had been lost and invalid data was being read back. The use of FIVIT also allowed the user to turn the POR bypass to either 'ON' or 'OFF', hence enabling or disabling the POR.

The cross section curves for parameters of interest are displayed in the following graphs (Fig. 5 – 8).

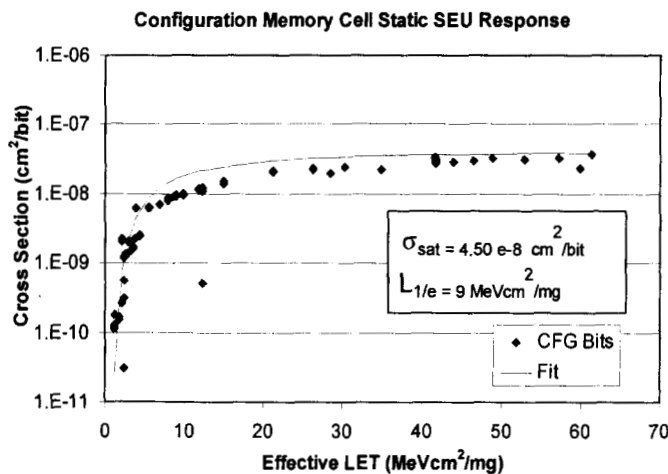


Figure 5: Cross-section vs. effective LET for configuration memory cells.

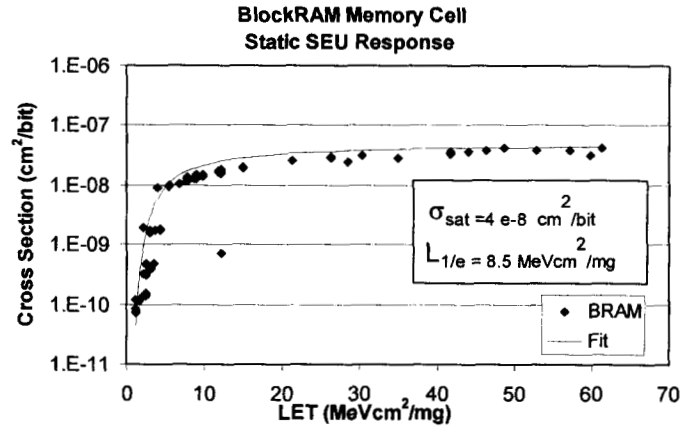


Figure 6: Cross-section vs. effective LET for block RAM memory cells.

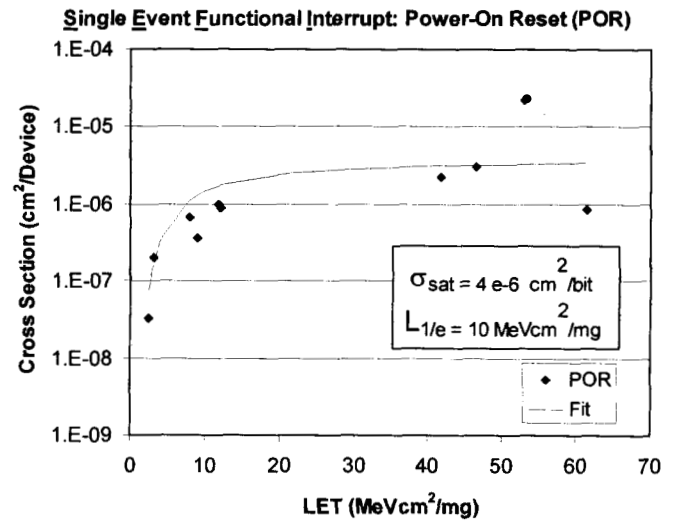


Figure 7: Cross-section vs. effective LET for POR SEFIs.

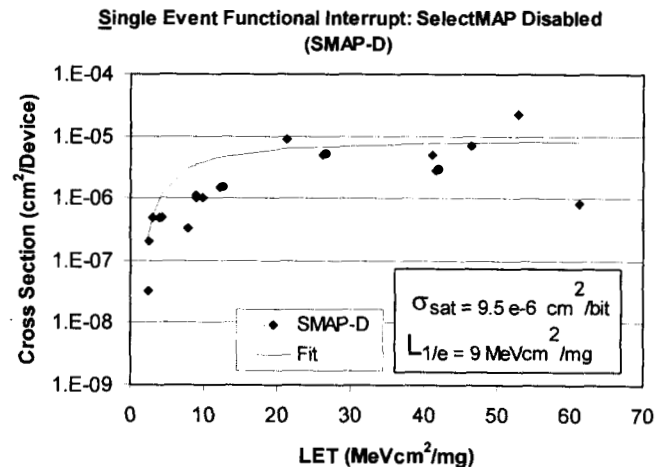


Figure 8: Cross-section vs. effective LET for SelectMap SEFIs.